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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/464,297	12/15/1999	SHELDON ARONOWITZ	99-039	7342

24319 7590 10/22/2003

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EXAMINER	
VINH, LAN	18

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/464,297	Applicant(s) ARONOWITZ ET AL.	
	Examiner Lan Vinh	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,7,9-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,7,9-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 9/5/2003 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/464,297 is acceptable and a RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 7, 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over McInerney et al (US 4,690,746) in view of Cohen et al (US 6,346,489)

McInerney discloses a process for etching a fixed thickness of silicon dioxide/oxide from a silicon dioxide/oxide layer formed on a semiconductor substrate in a process chamber 15 /etching apparatus. This process comprises the steps of:

exposing a silicon dioxide/oxide surface D of an integrated circuit structure on a semiconductor substrate 61 to a plasma generated by a gas mixture of N_2O/ argon/ SiH_4 , the gas mixture having a flow rate of 700 sccm/200sccm/50 sccm (col 4, lines 4-9; fig. 7), which reads on exposing a silicon oxide surface of an integrated circuit on a semiconductor substrate to a plasma consisting essentially of a nitrogen plasma. Fig. 7

of McInerney also shows that the plasma is generated by a RF power source of 900 watts (overlaps the claimed range of 250-1000 watts)

maintaining on the semiconductor substrate a DC bias from a RF matching network 21 at a voltage/energy/power level of from above zero up to a voltage/power level during the exposure/etching of the silicon dioxide/oxide to the gas mixture of N_2O/ argon/ SiH_4. Fig. 2 and fig. 10 shows the DC bias is from above zero to a level below 900 watts/the level at which sputtering of the substrate would commence (as seen in fig. 7), which reads on maintaining on the semiconductor substrate a DC bias from a second RF power source at power level of from above zero up to a voltage/power level just below a level at which sputtering of the substrate material would commence during the exposure of the silicon oxide to a plasma consisting essentially of nitrogen. McInerney also discloses etching a silicon dioxide having a thickness of 5100 angstroms from step 17 to a thickness of 3500 angstroms at step 23 (col 5, lines 9-35, fig. 10 shows that the DC bias increases during the etching step), which reads on removing a fixed thickness of silicon oxide from the silicon oxide region of uniform thickness leaving a silicon oxide layer having a thinner regions of uniform thickness, with the silicon oxide thickness removed during the etching step dependent on the power level of the DC bias on the semiconductor substrate .

McInerney differs from the instant claimed inventions as per claims 4 and 11 by maintaining a DC bias from a RF source instead of a RF bias.

However, Cohen, in a method of precleaning that minimize damage to low k dielectric layer, discloses that a bias RF power supply can help ignite and sustain the plasma and it can produced a DC bias voltage on the pedestal (col 3, lines 57-60)

Since McInerney discloses maintaining a negative DC bias (col 3, lines 28-30) from a RF source connected to the substrate holder, one skilled in the art would have found it obvious to modify McInerney's bias source by using a RF bias in view of Cohen's teaching because Cohen teaches that a bias RF power supply can produce a DC bias voltage on the pedestal that is most cases is negative relative to the plasma body (col 3, lines 58-61)

Regarding claims 7, 14, McInerney discloses generating the plasma by a first plasma generator 19 at a distance from the silicon dioxide surface formed on the semiconductor substrate (fig. 2)

Regarding claims 9, 15, McInerney discloses the etch rate occurs at 30 mT (col 6, lines 39-40), which overlaps the claimed range of 1-1000 mT

Regarding claim 12, fig. 10 of McInerney shows the DC bias range from above zero to about 100 volts.

The limitation of claim 13 has been discussed above.

Regarding claims 16, 18, McInerney discloses exposing successive oxide layers 63 to 70 formed on the semiconductor substrate to the gas mixture/nitrogen plasma (col 4, lines 29-31)

Regarding claim 17, fig. 6b of McInerney shows that the oxide layers are not masked during the etching.

4. Claims 19-20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over McInerney et al (US 4,690,746) in view of Cohen et al (US 6,346,489)

McInerney discloses a process for etching a fixed thickness of silicon dioxide/oxide from a silicon dioxide/oxide layer formed on a semiconductor substrate in a process chamber 15 /etching apparatus. This process comprises the steps of:

forming a silicon oxide layer D, in an integrated circuit on a semiconductor substrate (fig. 3)

placing the semiconductor substrate on an electrode/substrate support in a process chamber/etching chamber at a pressure of 30 mT (overlaps the claimed range of 1-500 mT) (col 6, lines 35-40)

exposing the unmasked silicon dioxide/oxide regions of an integrated circuit structure on a semiconductor substrate 61 to a plasma generated by a gas mixture of N_2O/ argon/ SiH_4 and remote RF generator 19 (fig. 2), the gas mixture having a flow rate of 700 sccm/200sccm/50 sccm (col 4, lines 4-9; fig. 7), which reads on exposing a silicon oxide surface of an integrated circuit on a semiconductor substrate to a plasma consisting essentially of a nitrogen plasma. Fig. 10 of McInerney also shows that the plasma is generated by a RF power source of from about 0.25 KW (250 W) to about 0.5 KW (500 W).

maintaining on the semiconductor substrate a DC bias from a RF matching network 21 (as seen in fig. 2) at a voltage/energy/power level of from above zero up to a voltage/power level during the exposure/etching of the silicon dioxide/oxide to the gas mixture of N_2O/ argon/ SiH_4. Fig. 10 shows the DC bias of about zero to 100 V/of about

50 V when the RF power is at about 250 W to 500 W. McInerney also discloses etching a silicon dioxide having a thickness of 5100 angstroms from step 17 to a thickness of 3500 angstroms at step 23 (col 5, lines 9-35, fig. 10 shows that the DC bias increases during the etching step), which reads on removing a fixed thickness of silicon oxide from the exposed silicon oxide region of uniform thickness leaving a thin silicon oxide layer/gate oxide portion having a thinner regions of uniform thickness, with the silicon oxide thickness removed during the etching step dependent on the power level of the DC bias on the semiconductor substrate.

McInerney differs from the instant claimed inventions as per claims 19 and 24 by maintaining a DC bias from a RF source instead of a RF bias.

However, Cohen, in a method of precleaning that minimize damage to low k dielectric layer, discloses that a bias RF power supply can help ignite and sustain the plasma and it can produced a DC bias voltage on the pedestal (col 3, lines 57-60)

Since McInerney discloses maintaining a negative DC bias (col 3, lines 28-30) from a RF source connected to the substrate holder, one skilled in the art would have found it obvious to modify McInerney's bias source by using a RF bias in view of Cohen's teaching because Cohen teaches that a bias RF power supply can produce a DC bias voltage on the pedestal that is most cases is negative relative to the plasma body (col 3, lines 58-61)

The limitation of claims 20, 22, 23 have been discussed above.

Response to Arguments

5. Applicant's arguments with respect to claims 4, 7, 9-20, 22-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703 305-2667. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

LV
October 15, 2003